查询CAT28C257HN-12T供应商

Advanced

# CAT28C257

## 256K-Bit CMOS PARALLEL E²PROM

## FEATURES

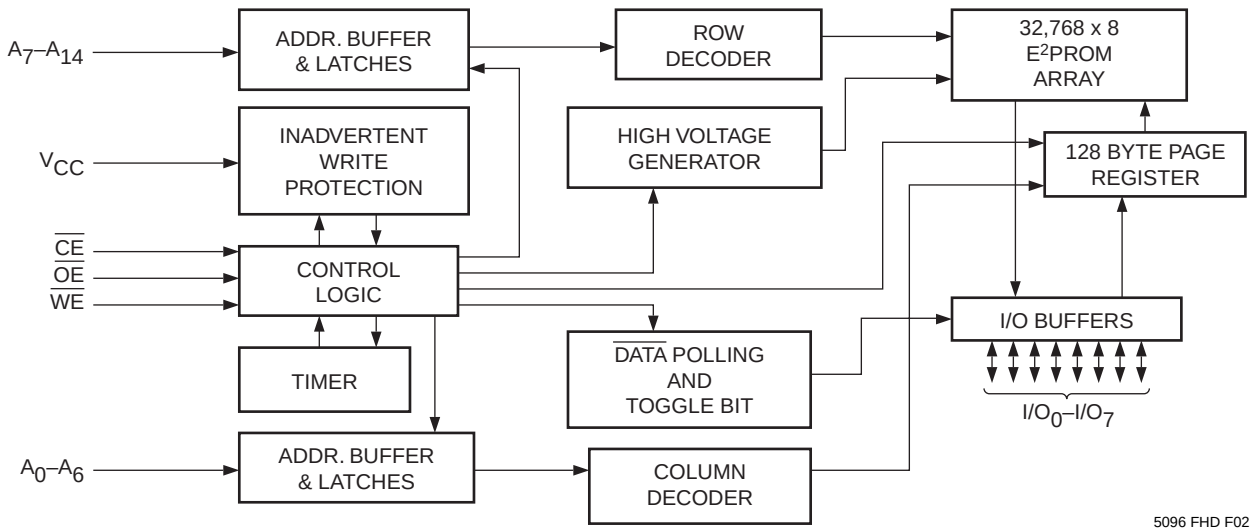
- **Fast Read Access Times: 90/120/150 ns**
- **Low Power CMOS Dissipation:**
  - **–Active: 25 mA Max.**
  - **–Standby: 150 μA Max.**
- **Simple Write Operation:**
  - **–On-Chip Address and Data Latches**
  - **–Self-Timed Write Cycle with Auto-Clear**
- **Fast Write Cycle Time:**
  - **–5ms Max**
- **CMOS and TTL Compatible I/O**
- **Automatic Page Write Operation:**
  - **–1 to 128 Bytes in 5ms**
  - **–Page Load Timer**
- **End of Write Detection:**
  - **–Toggle Bit**
  - **–$\overline{\text{DATA}}$ Polling**
- **Hardware and Software Write Protection**
- **100,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial, Industrial and Automotive Temperature Ranges**

## DESCRIPTION

The CAT28C257 is a fast, low power, 5V-only CMOS Parallel E²PROM organized as 32K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and $V_{CC}$ power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C257 features hardware and software write protection.

The CAT28C257 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 100 years. The device is available in JEDEC approved 28-pin DIP, 28-pin TSOP or 32-pin PLCC packages.

## BLOCK DIAGRAM

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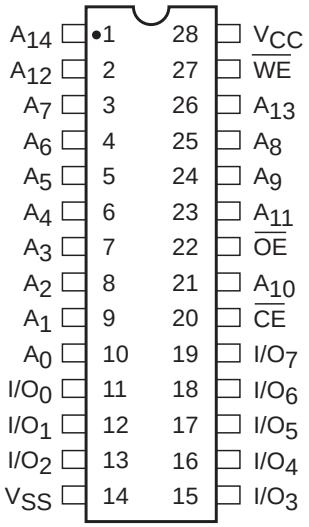
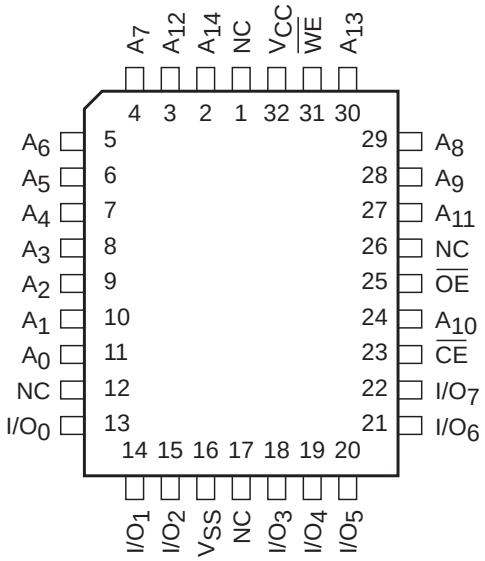
Doc. No. 25073-00 2/98

## PIN CONFIGURATION

**DIP Package (P)**




**PLCC Package (N)**

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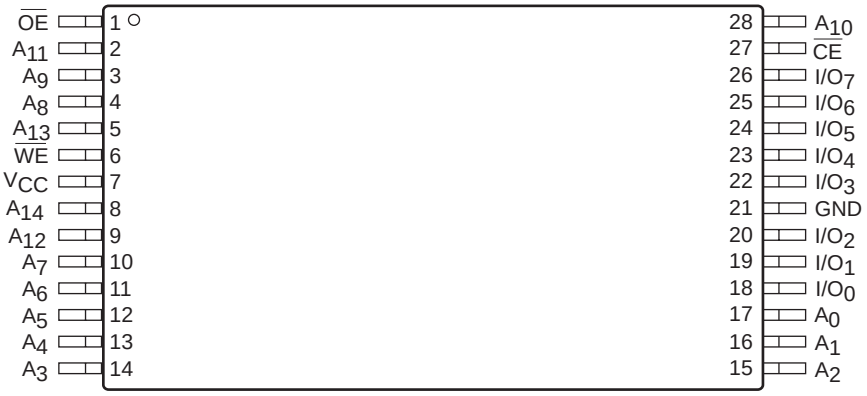
**TSOP Package (8mm X 13.4mm) (T13)**




28C257 F03

## PIN FUNCTIONS

| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| $A_0$–$A_{14}$ | Address Inputs | $\overline{WE}$ | Write Enable |
| $I/O_0$–$I/O_7$ | Data Inputs/Outputs | $V_{CC}$ | 5V Supply |
| $\overline{CE}$ | Chip Enable | $V_{SS}$ | Ground |
| $\overline{OE}$ | Output Enable | NC | No Connect |

## ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with
Respect to Ground(2) ..... –2.0V to +$V_{CC}$ + 2.0V

$V_{CC}$ with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation
Capability (Ta = 25°C) ..... 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

## *COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

### RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Min. | Max. | Units | Test Method |
|---|---|---|---|---|---|
| $N_{END}$(1) | Endurance | $10^4$ or $10^5$ | | Cycles/Byte | MIL-STD-883, Test Method 1033 |
| $T_{DR}$(1) | Data Retention | 100 | | Years | MIL-STD-883, Test Method 1008 |
| $V_{ZAP}$(1) | ESD Susceptibility | 2000 | | Volts | MIL-STD-883, Test Method 3015 |
| $I_{LTH}$(1)(4) | Latch-Up | 100 | | mA | JEDEC Standard 17 |

### D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = 5V ±10%, unless otherwise specified.

| Symbol | Parameter | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $I_{CC}$ | $V_{CC}$ Current (Operating, TTL) | | | 30 | mA | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, f=6MH$_z$<br>All I/O’s Open |
| $I_{CCC}$(5) | $V_{CC}$ Current (Operating, CMOS) | | | 25 | mA | $\overline{CE}$ = $\overline{OE}$ = $V_{ILC}$, f=6MH$_z$<br>All I/O’s Open |
| $I_{SB}$ | $V_{CC}$ Current (Standby, TTL) | | | 1 | mA | $\overline{CE}$ = $V_{IH}$, All I/O’s Open |
| $I_{SBC}$(6) | $V_{CC}$ Current (Standby, CMOS) | | | 150 | µA | $\overline{CE}$ = $V_{IHC}$,<br>All I/O’s Open |
| $I_{LI}$ | Input Leakage Current | –10 | | 10 | µA | $V_{IN}$ = GND to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | –10 | | 10 | µA | $V_{OUT}$ = GND to $V_{CC}$,<br>$\overline{CE}$ = $V_{IH}$ |
| $V_{IH}$(6) | High Level Input Voltage | 2 | | $V_{CC}$ +0.3 | V | |
| $V_{IL}$(5) | Low Level Input Voltage | –0.3 | | 0.8 | V | |
| $V_{OH}$ | High Level Output Voltage | 2.4 | | | V | $I_{OH}$ = –400µA |
| $V_{OL}$ | Low Level Output Voltage | | | 0.4 | V | $I_{OL}$ = 2.1mA |
| $V_{WI}$ | Write Inhibit Voltage | 3.5 | | | V | |

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ +0.5V, which may overshoot to $V_{CC}$ +2.0V for periods of less than 20 ns.
(3) Output shorted for no more than one second. No more than one output shorted at a time.
(4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to $V_{CC}$ +1V.
(5) $V_{ILC}$ = –0.3V to +0.3V.
(6) $V_{IHC}$ = $V_{CC}$ –0.3V to $V_{CC}$ +0.3V.

**MODE SELECTION**

| Mode | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | I/O | Power |
|---|---|---|---|---|---|
| Read | L | H | L | $D_{OUT}$ | ACTIVE |
| Byte Write ($\overline{WE}$ Controlled) | L | ⎍ | H | $D_{IN}$ | ACTIVE |
| Byte Write ($\overline{CE}$ Controlled) | ⎍ | L | H | $D_{IN}$ | ACTIVE |
| Standby, and Write Inhibit | H | X | X | High-Z | STANDBY |
| Read and Write Inhibit | X | H | H | High-Z | ACTIVE |

**CAPACITANCE** $T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5V

| Symbol | Test | Max. | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$(1) | Input/Output Capacitance | 10 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(1) | Input Capacitance | 6 | pF | $V_{IN}$ = 0V |

**A.C. CHARACTERISTICS, Read Cycle**

$V_{CC}$=5V ± 10%, Unless otherwise specified

| | | 28C257-90 | | 28C257-12 | | 28C257-15 | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max** | **Min.** | **Max.** | **Units** |
| $t_{RC}$ | Read Cycle Time | 90 | | 120 | | 150 | | ns |
| $t_{CE}$ | $\overline{CE}$ Access Time | | 90 | | 120 | | 150 | ns |
| $t_{AA}$ | Address Access Time | | 90 | | 120 | | 150 | ns |
| $t_{OE}$ | $\overline{OE}$ Access Time | | 40 | | 50 | | 70 | ns |
| $t_{LZ}$(1) | $\overline{CE}$ Low to Active Output | 0 | | 0 | | 0 | | ns |
| $t_{OLZ}$(1) | $\overline{OE}$ Low to Active Output | 0 | | 0 | | 0 | | ns |
| $t_{HZ}$(1)(2) | $\overline{CE}$ High to High-Z Output | | 40 | | 50 | | 50 | ns |
| $t_{OHZ}$(1)(2) | $\overline{OE}$ High to High-Z Output | | 40 | | 50 | | 50 | ns |
| $t_{OH}$(1) | Output Hold from Address Change | 0 | | 0 | | 0 | | ns |

**Power-Up Timing**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{PUR}$ | Power-Up to Read | | 100 | µs |
| $t_{PUW}$ | Power-Up to Write | 5 | 10 | ms |

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

### A.C. CHARACTERISTICS, Write Cycle

$V_{CC}$=5V±10%, unless otherwise specified

| Symbol | Parameter | 28C257-90 | | 28C257-12 | | 28C257-15 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WC}$ | Write Cycle Time | | 5 | | 5 | | 5 | ms |
| $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | 50 | | 50 | | ns |
| $t_{CS}$ | $\overline{CE}$ Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{CH}$ | $\overline{CE}$ Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{CW}$(3 | $\overline{CE}$ Pulse Time | 100 | | 100 | | 100 | | ns |
| $t_{OES}$ | $\overline{OE}$ Setup Time | 0 | | 0 | | 0 | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{WP}$(3) | $\overline{WE}$ Pulse Width | 100 | | 100 | | 100 | | ns |
| $t_{DS}$ | Data Setup Time | 50 | | 50 | | 50 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | ns |
| $t_{INIT}$(1) | Write Inhibit Period After Power-up | 5 | 10 | 5 | 10 | 5 | 10 | ms |
| $t_{BLC}$(1)(4) | Byte Load Cycle Time | 0.1 | 100 | 0.1 | 100 | 0.1 | 100 | µs |

**Figure 1. A.C. Testing Input/Output Waveform(2)**

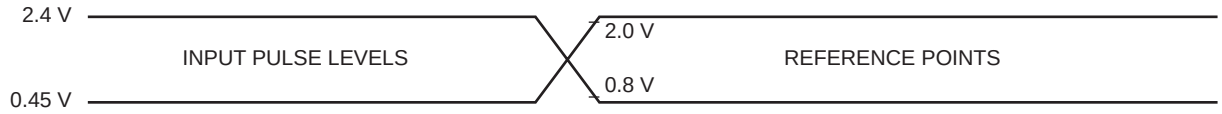



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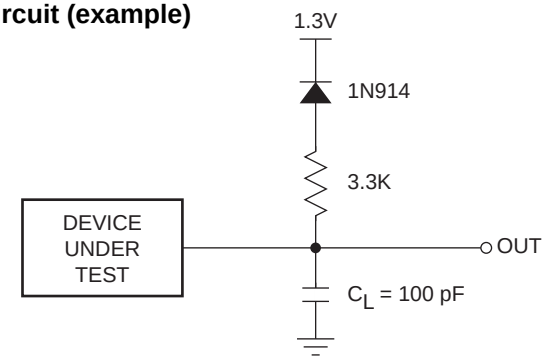
**Figure 2. A.C. Testing Load Circuit (example)**

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$C_L$ INCLUDES JIG CAPACITANCE

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Input rise and fall times (10% and 90%) < 10 ns.
(3) A write pulse of less than 20ns duration will not initiate a write cycle.
(4) A timer of duration $t_{BLC}$ max. begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within $t_{BLC}$ max. stops the timer.

## DEVICE OPERATION

### Read

Data stored in the CAT28C257 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set to a high impedance state when either $\overline{CE}$ or $\overline{OE}$ goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

### Byte Write

A write cycle is executed when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be initiated using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 5 ms.

**Figure 3. Read Cycle**

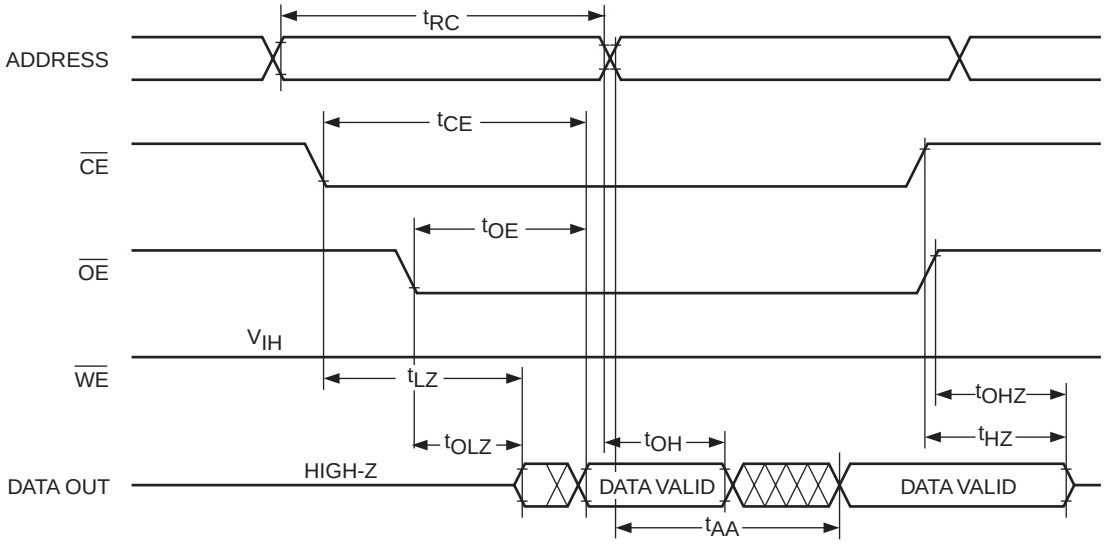


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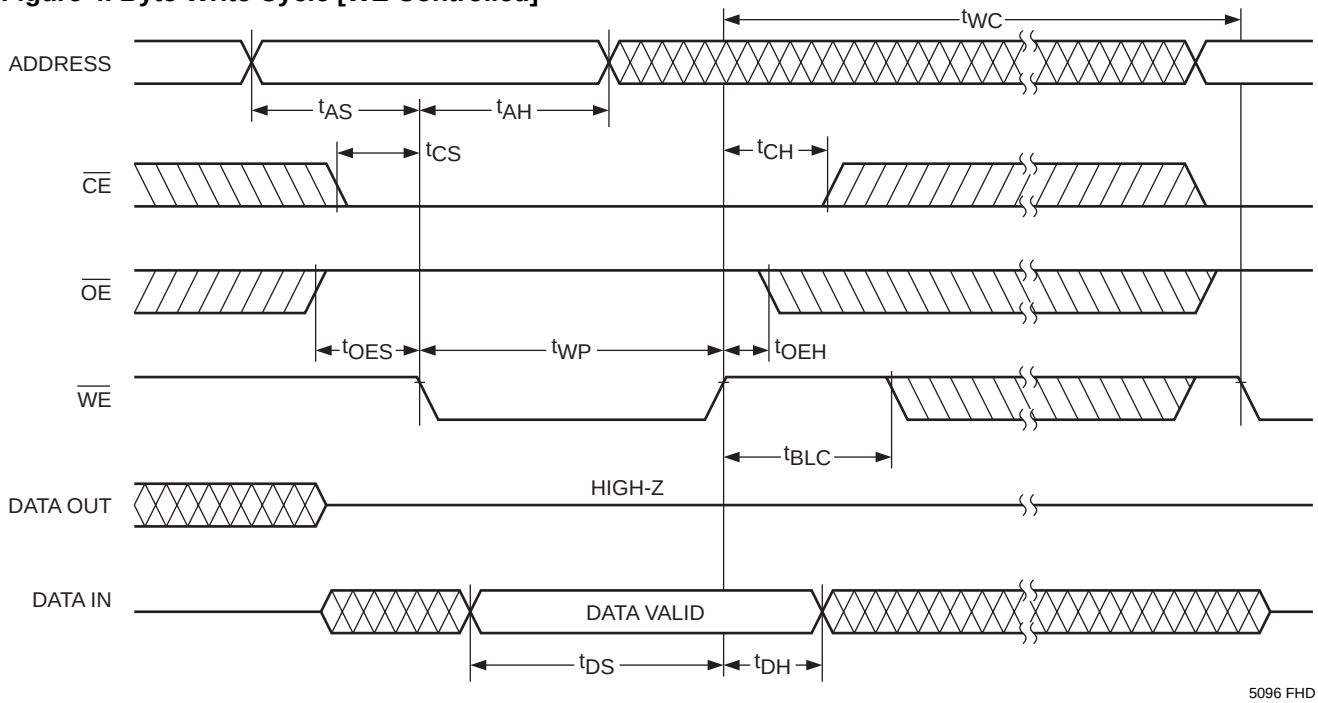
**Figure 4. Byte Write Cycle [$\overline{WE}$ Controlled]**

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### Page Write

The page write mode of the CAT28C257 (essentially an extended BYTE WRITE mode) allows from 1 to 128 bytes of data to be programmed within a single $E^2$PROM write cycle. This effectively reduces the byte-write time by a factor of 128.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for $t_{WP}$, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a128 byte temporary buffer. The page address where data is to be written, specified by bits $A_7$ to $A_{14}$, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits $A_0$ to $A_6$ (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within $t_{BLC\,MAX}$ of the falling edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within $t_{BLC\,MAX}$.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of $t_{BLC\,MAX}$ for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

**Figure 5. Byte Write Cycle [$\overline{CE}$ Controlled]**

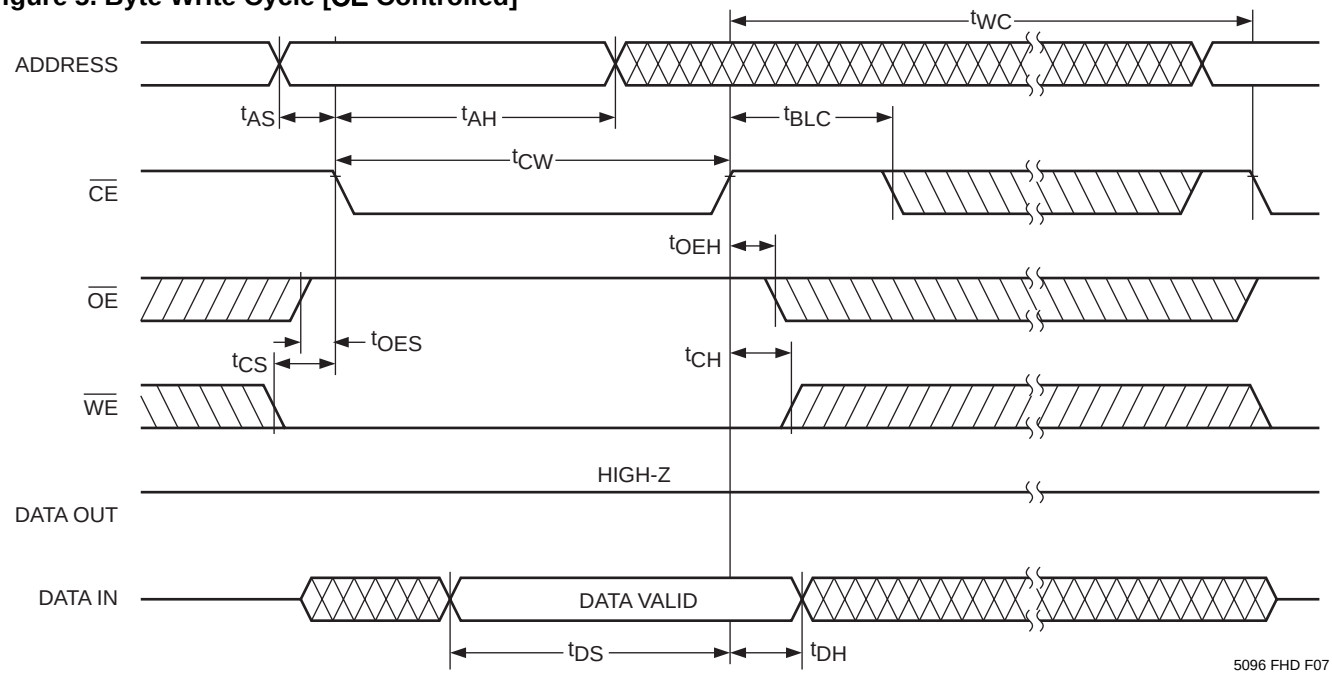
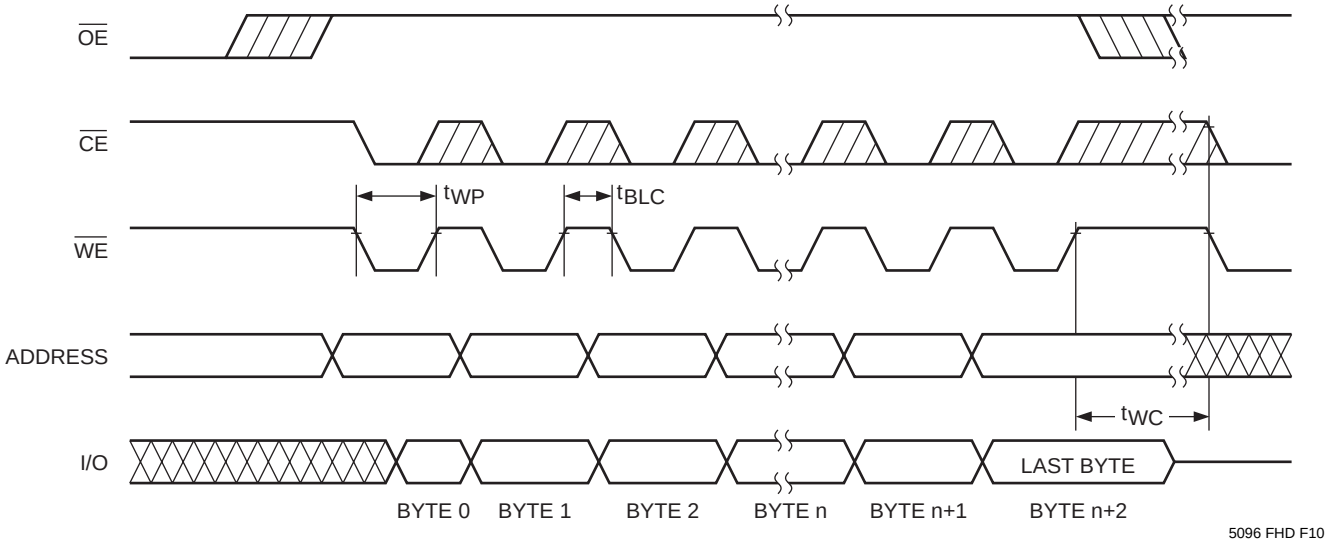



**Figure 6. Page Mode Write Cycle**



### $\overline{\text{DATA}}$ Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of write cycle. Once a byte write or page write cycle is initiated, attempting to read the last byte written will output the complement of that data on $I/O_7$ ($I/O_0$–$I/O_6$ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle, all I/O's will output true data during a read cycle.

### Toggle Bit

In addition to the $\overline{\text{DATA}}$ Polling feature of the CAT28C257, the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, reading data from the device will result in $I/O_6$ toggling between one and zero. However, once the write is complete, $I/O_6$ stops toggling and valid data can be read from the device.

**Figure 7. $\overline{\text{DATA}}$ Polling**

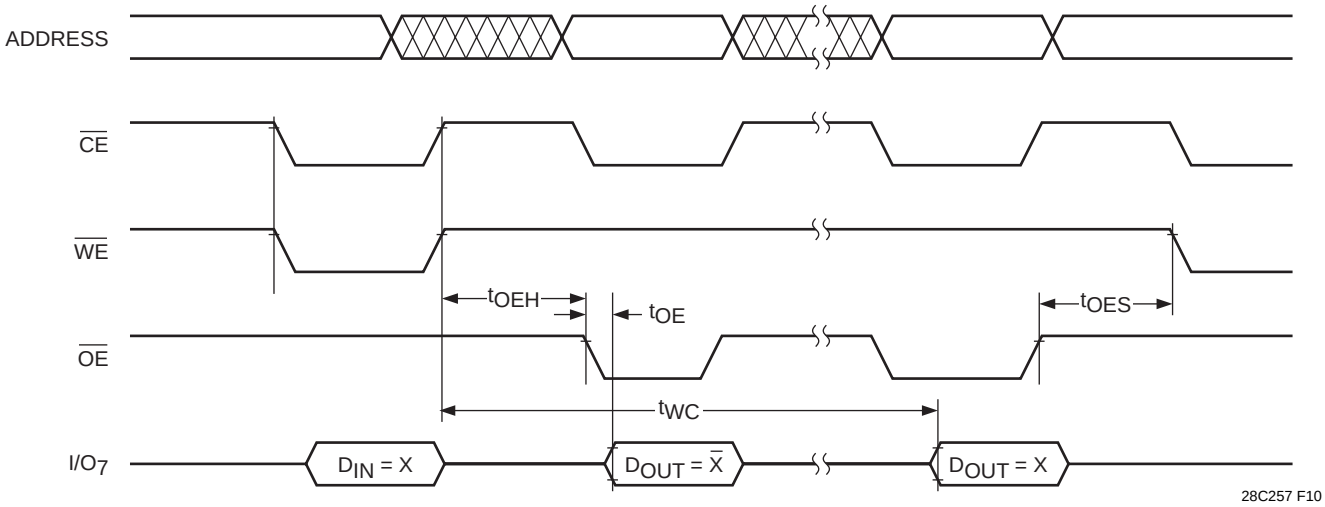
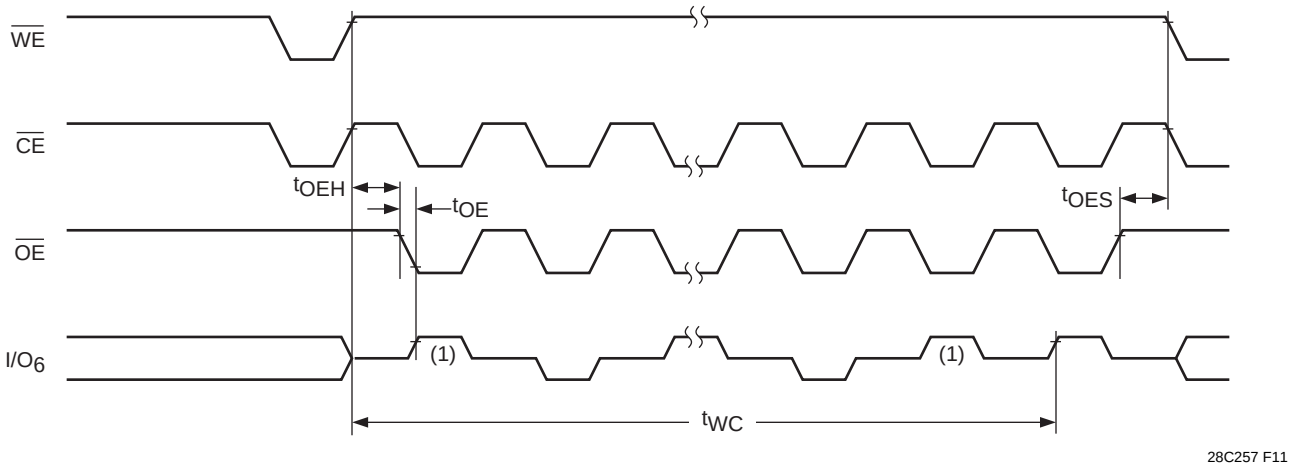



**Figure 8. Toggle Bit**




Note:
(1) Beginning and ending state of $I/O_6$ is indeterminate.

## HARDWARE DATA PROTECTION

The following is a list of hardware data protection features that are incorporated into the CAT28C257.

(1) $V_{CC}$ sense provides for write protection when $V_{CC}$ falls below 3.5V min.

(2) A power on delay mechanism, $t_{INIT}$ (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after $V_{CC}$ has reached 3.5V min.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

## SOFTWARE DATA PROTECTION

The CAT28C257 features a software controlled data protection scheme which, once enabled, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C257 is in the standard operating mode).

**Figure 9. Write Sequence for Activating Software Data Protection**

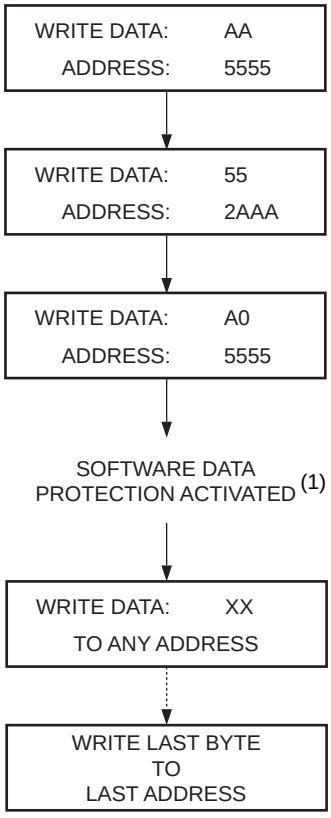



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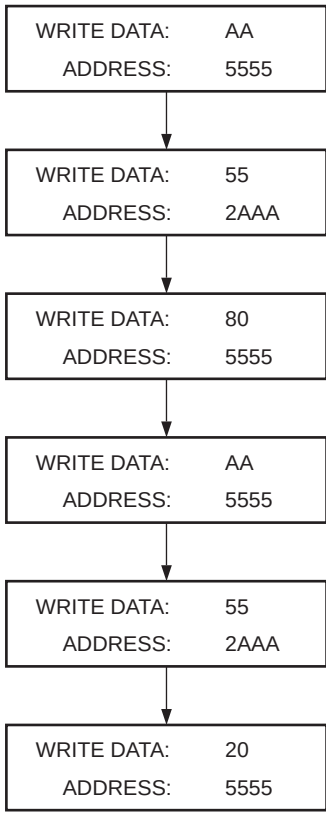
**Figure 10. Write Sequence for Deactivating Software Data Protection**

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Note:
(1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within $t_{BLC}$ Max., after SDP activation.

To activate the software data protection, the device must be sent three write commands to specific addresses with specific data (Figure 9). This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications (Figure 11). Once this is done, all subsequent byte or page writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the device with an $E^2$PROM programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (Figure 10) will reset the internal protection circuitry, and the device will return to standard operating mode (Figure 12 provides reset timing). After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

**Figure 11. Software Data Protection Timing**

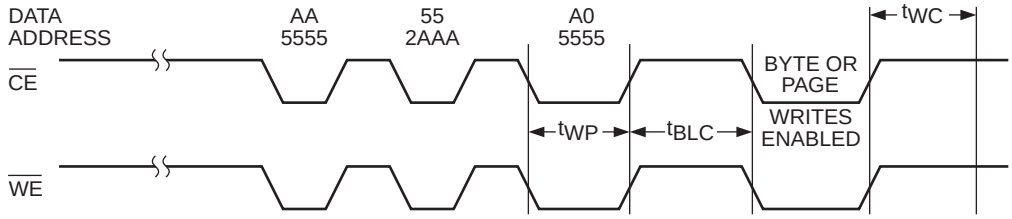


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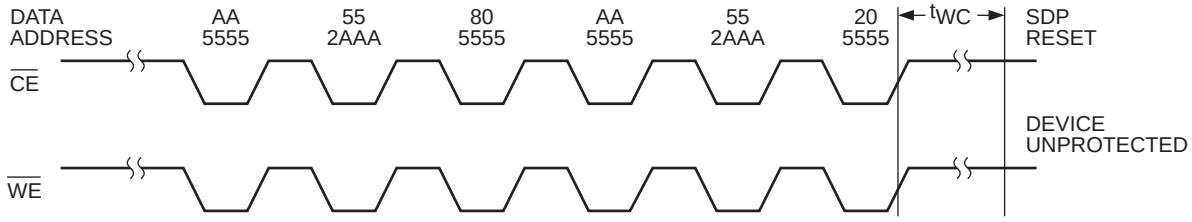
**Figure 12. Resetting Software Data Protection Timing**

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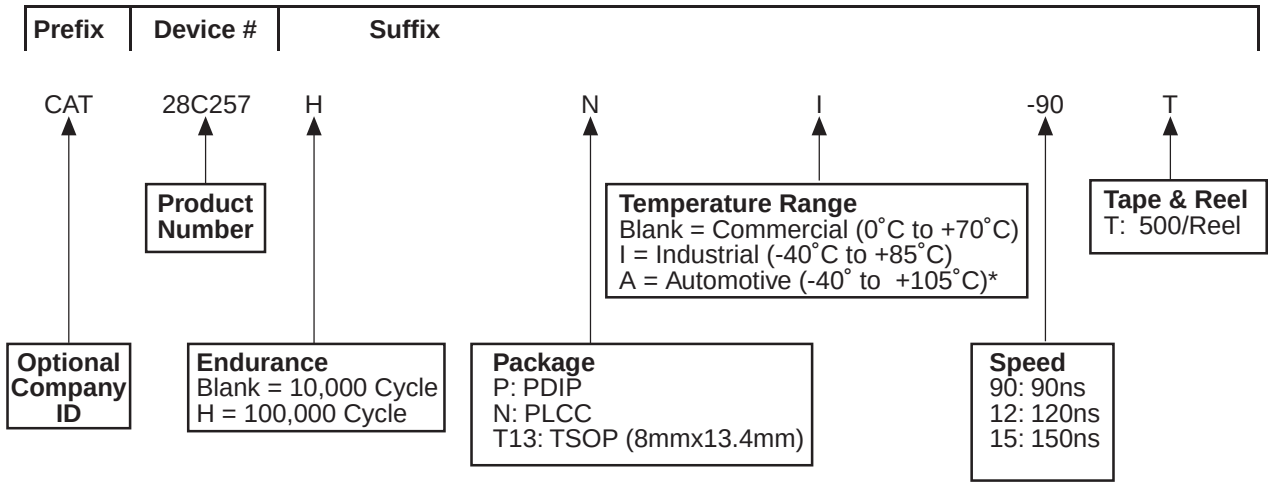
**ORDERING INFORMATION**




* -40˚C to +125˚C is available upon request

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Notes:

(1) The device used in the above example is a CAT28C257HNI-90T (100,000 Cycle Endurance, PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).